

# Design and Performance of FDL buffers in Optical Switches\*

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**Abstract**—A key technique for reducing packet blocking in optical switches is by temporarily buffering packets in fiber delay lines (FDLs). The packet blocking probability depend on the FDLs design as well as on how packets are scheduled to the FDL buffers. This study compares between the blocking probabilities of the following design and buffer scheduler options: (i) input vs output port FDLs; (ii) shared vs port-dependent FDLs; (iii) forward vs feedback FDLs; (iv) variable vs fixed size FDLs; and (v) FIFO vs non-overlapping buffer schedulers. The comparison results reveals several interesting facts. The first one is that feedback FDL design can reduce the number of required buffers by 75% compared with a forward FDL design. Another observed fact is that fixed-size FDLs is very wasteful, specifically, the length of a fixed size FDL has no affect on the blocking probability. The third observation is that a non-overlapping buffer scheduler can reduce the number of required FDLs by 30% compared with a FIFO scheduler.

**Index Terms**—All optical networks, optical switches, fiber delay line, blocking probability.

## I. INTRODUCTION

THE advancement of optical technology in recent years positions the all-optical network (AON) as a viable option for next-generation communication networks. Being able to send a data-carrying optical signals for thousands of kilometers, through many transparent optical switches without conversion to the electronic domain is the key feature defining an AON.

One of the important elements for reducing packet blocking in an optical switch is temporarily buffering in fiber delay lines (FDLs). The FDLs buffer design and the packet scheduling to the buffers play crucial roles and greatly affect the blocking probability. The current paper concerns with the performance comparison between various design and schedule options. The focus is restricted to the blocking probability aspect and ignores the architectural implementation cost.

FDL design options can be classified as follows:

- Input vs output port FDLs.
- Shared vs port-dependent FDLs.
- Forward vs feedback FDLs.
- Variable vs fixed size FDLs.
- Simple vs non-overlapping buffer scheduler.

A simple buffer scheduling is basically a FIFO scheduler and a non-overlapping buffer scheduler is a scheduler ensuring that

the packets exiting from the FDLs do not contend for the same output ports.

The architectural pros and cons of the various design options are explained in [3] and in the references therein. It should be noted that FDL buffers are different than electronic buffers since light photons keep propagating in the FDLs requiring extremely long and bulky FDL buffers. This hard constraint have two design implication. One is the FDL lengths and the other is the packet contention resolution properties.

Storing capability is clearly related to the total FDL lengths. FDL lengths, however, has almost no affect on contention resolution. Packet feedback capability and FDL length variability, on the other hand, are expected to be key factors in the contention resolution process. An interesting and important design question is how much impact each design aspect has on the packet blocking probability?

Packet scheduling to the various FDLs is strongly related to contention resolution since it determines the time when packets are available for switching (FDL exit time). For instance, exit time overlapping between packets destined to the same output ports will clearly result in another contention. Thus, another interesting and important design question is the impact of a packet scheduler on the blocking probability.

It is well known that buffering in the output ports outperforms buffering in the input ports and shared buffers outperforms port-dependent buffers. Therefore, the performance comparison between various options of feedback/forward, FDL lengths and buffer schedulers will be studied herein.

## II. THE SWITCH MODEL

An  $N \times N$  all optical switch with  $K$  shared FDLs placed at the output ports are considered. The optical packets are assumed to be of a fixed length and the time axis to be slotted and aligned with the packet length. The switching is synchronized and packets are available for switching or buffering at the beginning of each time slot. FDL  $k$  can contain up to  $L(k)$  packets in ‘time cells’  $1, \dots, L(k)$ . A packet enters at time cell  $L(k)$  and propagates along the FDL at a constant speed (about 200,000 km/sec) and exits at time cell one. The FDL propagation time is  $L(k)$  time slots.

New packets arrive from the input ports according to a renewal Bernoulli process and become available for switching or buffering at the beginning of each time slot. A packet arriving from input port  $n$  is destined to any output port  $n' \neq n$  with equal probability of  $1/(N-1)$ . The overall offered load to each output port from all input ports is denoted by  $\rho \leq 1$ .

Let  $\mathbf{X}(t) = (X_1(t), \dots, X_N(t))$  be the number of packets arriving at the beginning of time slot  $t = 1, 2, \dots$ , where  $X_i(t)$

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denotes the number of packets destined to output  $i$ . The new arrivals and the every packet in the first time cell of each FDL are contending on the output ports. If the number of packets contending for output port  $n$ ,  $n = 1, \dots, N$ , is greater than one, a *switching scheduler* decides which one is switched out and a *buffering scheduler* decides which packet is buffered and in which FDL.

With forward FDLs, contending packets arriving from the FDLs cannot re-buffer and, if not scheduled by the switching scheduler, they are lost. A straightforward packet identity swapping argument reveals that the switching scheduler does not affect the blocking probability. However, it does affect the packet queuing delay. FIFO, LIFO QoS-based priority, etc. switching scheduler can be implemented since packets headers must be extracted anyway for the switching task. The buffering scheduler, on the other hand, does affect the blocking probability and therefore important to understand.

The blocking probabilities of various FDL designs and buffering schedulers are studied via simulation. Simulating a synchronized time slotted switch with fixed packet length is a simple and a very fast mechanism. Since the performance comparison concern with very small blocking probabilities ( $10^{-4} - 10^{-6}$ ), special consideration are given in the simulator to the running time.

Previous performance evaluation of switches with various designs have been studied via approximated analysis, e.g., [1] and [2]. Precise analysis of practical FDL designs with shared buffers are mathematically intractable whereas their approximated analysis would require validation by simulation. In the present paper, performance evaluation is done only by simulation.

### III. FORWARD VS FEEDBACK WITH SHARED FDLs

A switch with forward FDLs is simpler and less costly compared with a switch with feedback FDLs. The former requires an  $N \times (N + K)$  switching fabric whereas the latter requires an  $(N + K) \times (N + K)$  fabric [4]. Since feedback FDLs have more flexibility in resolving contending packets, it is important to find the saving in FDLs for achieving a target blocking probability.

To this end, the two designs are compared using variable FDL lengths with  $L(k) = k$  cells,  $k = 1, \dots, K$ , FIFO switching scheduler and the following buffering scheduler. In the feedback design, buffering priority is given to buffered packets (implied from the FIFO regime). Also, in both designs, preventing *time slot overlapping* is a main consideration. By time slot overlapping it is meant that at least two packets destined to the same output port will exit the FDLs at the same time.

With the forward FDL switch, time slot overlapping is strictly prohibited since it results in sure blocking. Therefore, at any event where  $j$  packets destined to port  $n$  require buffering, each FDL  $k$  is observed sequentially at time cell  $L(k)$  to verify if it is free and all the corresponding time cells in FDLs  $k' > k$  contain packets also destined to port  $n$ . If such time overlapping does not exist, the packet is buffered. Note that packets are buffered one by one and independently.

When the search over all FDLs is complete, the unbuffered packets are blocked. Packets are buffered so as to preserve FIFO upon their exit from the FDLs.

With the feedback FDL switch, buffering priority is given to buffered packets and scheduling is done in two phases. The first phase is overlapping-free, as described above, starting with the buffered packets and continuing with the new packets. The second phase buffers the remaining packets at any free entry time cell  $L(k)$ ,  $k = 1, \dots, K$ . All the rest are blocked. The reason for executing the second phase rather than blocking is that contention resolution can be deferred to subsequent time slots.

The minimum number of FDLs required to meet threshold blocking probabilities of  $10^{-4}$  and  $10^{-6}$  with feedback and forward FDLs with  $N$  input and output ports as a function of the load level  $\rho$  is depicted in Figure 1.

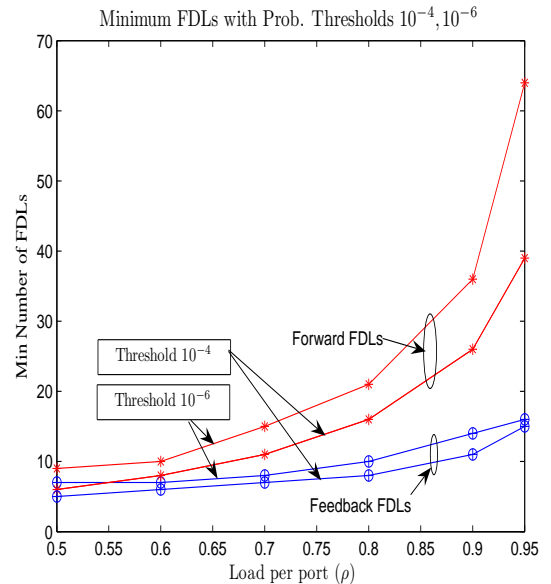


Fig. 1. Minimum number of shared FDLs in a switch with 8 output ports requiring blocking probabilities of  $10^{-4}$  and  $10^{-6}$ .

Generally, a switch should be designed to address high loads and very small blocking probabilities. Therefore, the most valuable information concerns with threshold  $10^{-6}$  and load  $\rho = 0.95$ . A switch with forward FDLs requires 64 compared with 16 required with feedback FDLs. A reduction of 75% in the number of FDLs is significant and can compensate the extra cost required for feedback FDLs implementation. It certainly reduces the size of the switch.

### IV. VARIABLE VS FIXED SIZE FEEDBACK SHARED FDLs

Since feedback FDLs may result in arbitrary packet delay during the contention resolution phase, it is further interesting to investigate the impact of reducing the FDL lengths. To this end, a comparison is made between a feedback shared FDLs switch with variable FDL lengths and fixed length. For each offer load,  $\rho$ , the number of FDLs used in both designs equals the minimum number achieving the threshold probability of  $10^{-6}$ .

The blocking probabilities as a function of the fixed FDL lengths is depicted in Figure 2. It is quite surprising to notice that for each offered load the blocking probabilities is almost flat with respect to the FDL length and is significantly higher compared with variable length FDLs. Particularly, the blocking probabilities with fixed FDL length for  $\rho = 0.95$  is 0.069 for 16 FDLs, each of length 16, compared with at least  $10^{-6}$  for 16 FDLs with length varying from 1 to 16. Namely, in spite of the larger buffer capacity, the blocking probability is significantly higher.

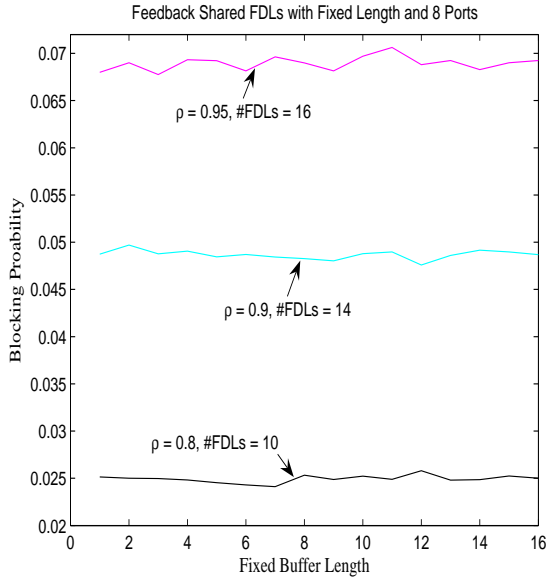


Fig. 2. Blocking probabilities in a feedback shared FDLs switch with 8 output ports and fixed FDL lengths as a function of the FDL length for  $\rho = 0.8, 0.9, 0.95$ .

This surprising flatness phenomenon can be explained by the stationary probability distribution of the packet port destinations in each time cell across the FDLs. Denote by  $\mathbf{Y}^i(t) = (Y_1^i(t), \dots, Y_K^i(t))$  the port labels at FDL time cell  $i$  and time slot  $t$ , where  $Y_k^i(t)$  is the port label in the  $i$ -th time cell of FDL  $k$  at time slot  $t$ .

Let  $p^i(t) = Pr(\mathbf{Y}^i(t) = \mathbf{y}^i(t))$ . Then, since packets propagate deterministically along the FDLs, for every time slot  $t$ ,

$$p^i(t+1) = p^{i+1}(t), \quad i = 1, \dots, L-1,$$

where  $L$  is the FDL length.

Thus, letting  $t$  approach infinity, the stationary marginal distributions  $\{p^i(t)\}$  satisfy

$$p^i(t) = p^j(t), \quad \forall i, j. \quad (1)$$

The interpretation of (1) is that the output port distribution,  $p^1(t)$ , is determined by  $p^L(t)$  regardless of how many circulation has been made. Although feedback helps in reducing the blocking probability, as demonstrated in Figure 1, it is the spreading property at the entry time cells what makes the greatest impact.

## V. SHARED VS PORT-DEPENDENT FDLs

Shared FDLs are more complex and expensive to implement compared with port-dependent FDLs. Thus, it is interesting to study its relative performance merit.

With port-dependent FDLs it is suffice to consider a single output port along with its set of FDLs. Since feedback FDLs are significantly better than forward FDLs, only this design will be considered.

Figure 3 compares the total minimum number of shared FDLs to the minimum number per port with port-dependent FDLs in feedback FDLs. It can be observed that port-dependent design requires for each port almost the same total number of FDLs in shared FDL design. This phenomenon further supports the observation in Section IV that buffering capacity is secondary and significantly less important than the spreading property inherent in variable length FDLs. Namely, the large number of FDLs required for each port-dependent buffers, serves only the required spreading property. The extra storage capacity coming with it, is apparently wasted and is greatly utilized by the shared FDL design.

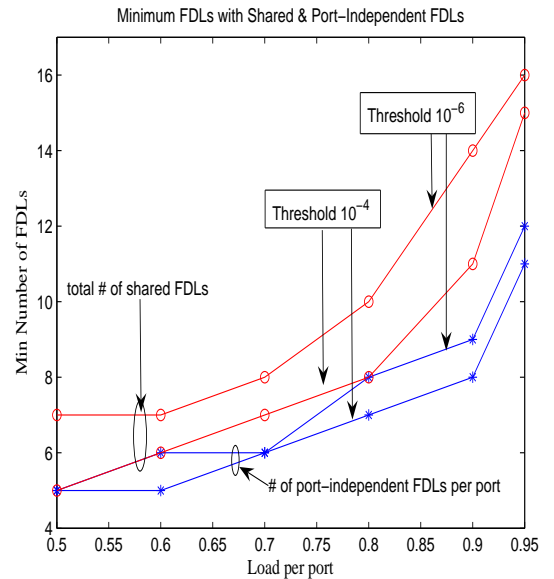


Fig. 3. Minimum total number of shared FDLs and minimum number of port-dependent FDLs per port, in a switch with 8 output ports requiring blocking probabilities of  $10^{-4}$  and  $10^{-6}$ .

## VI. SIMPLE VS NON-OVERLAPPING BUFFER SCHEDULER

The buffer scheduler used in Section III is a two-phase scheduler where the first phase schedule packets to FDLs so as to avoid contentions at exit. The second phase utilizes the rest of the available time cells in the FDLs. Such buffer scheduler is complex to implement.

Thus, it is of interest to investigate how the following simple buffer scheduler is performing compared with the complex one. With the simple scheduler, preference is also given to the buffered packets, and each one that cannot be switched out is feedback to its own FDL. New arrivals that cannot be switched out are buffered in the first available FDL.

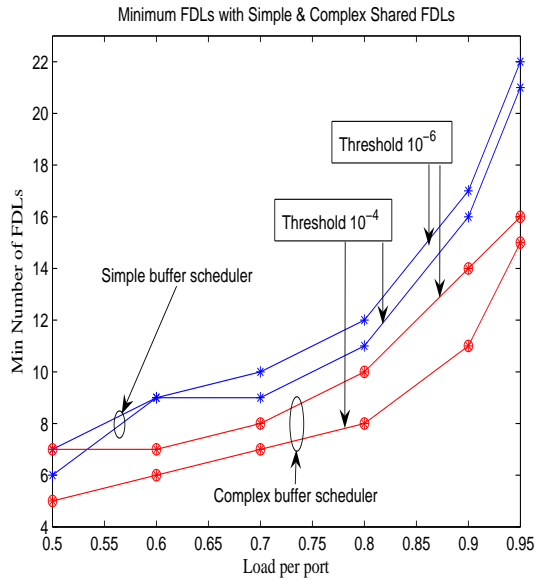


Fig. 4. Minimum number of shared FDLs in a switch with 8 output ports requiring blocking probabilities of  $10^{-4}$  and  $10^{-6}$ .

The minimum number of shared FDLs in a switch with 8 input and output ports for threshold blocking probabilities of  $10^{-4}$  and  $10^{-6}$  is depicted in 4. It can be observed that for  $\rho = 0.95$  and blocking probability threshold of  $10^{-6}$ , the simple scheduler requires 22 FDLs compared with 16 FDLs required by the complex scheduler, which is a 30% reduction.

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